

Technical Issues and Challenges in the Fabrication of a 144-Cell 500× Concentrating Photovoltaic Receiver

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Abstract - Concentrating Photovoltaics (CPV) aims to reduce the cost of photovoltaic applications by replacing part of the semiconductor material with a less expensive concentrating material. The significant increase in irradiance and the related reduction of semiconductor area introduce some criticisms that affect the design, fabrication and operating stages. The system needs to handle high power and current densities and high heat fluxes, without having repercussions on the cost, the size and the weight of the module.

The concentrating photovoltaic is an increasing market and a number of commercial companies has started or is starting to produce CPV receivers. Many papers have been published on the improvement in cell efficiency and on new system's design, but there is a lack of information about the manufacturing stage. An in depth investigation into benefits and weaknesses of assembly methods need to be carried out. This paper describes all the issues and the challenges faced during the fabrication of a novel large densely-packed system.

Index Terms — photovoltaic systems, prototypes, fabrication, printed circuits, integrated circuit packaging, power engineering and energy.

I. INTRODUCTION

The main aim of concentrating photovoltaics (CPV) is to reduce the amount of semiconductor material needed by replacing it with cheaper optical devices and, thus, increasing the density of the sunlight hitting the cells. This solution requires good thermal behavior, ability to provide a quick transfer of high power of waste heat, and good electrical performances, in order to generate electrical energy with high efficiency.

Multijunction (MJ) solar cells have recently reached record efficiencies of 44.7% [1]: the largest amount of incoming energy cannot be used yet and is still converted into heat, which lowers the performances of the system. The fabrication of a CPV system requires a balance between thermal and electrical performances both in the choice of the materials and components and in the execution of the manufacturing processes. The high electrical and power densities, the elevated insulation, the restricted surfaces and volumes of the components are concerns to be taken into account while designing and producing the system. Reliability, durability and cost of the CPV need to be considered as well [2]. All these issues increase the complexity of the development of a CPV

receiver: this case, the procedures used for common flat-PV or silicon cells cannot be always employed. In the last decade, the development of new CPV assemblies has been presented in many researches [3]–[5] and patents [6]–[8], but none have reported data or experiences on CPV manufacturing.

This paper illustrates all the fabrication stages of a novel 2.6 kW_p assembly for 500× CPV applications. This system is equipped with 144 MJ cells and two reflective geometries (Fig. 1): a primary 125× optics and a secondary 4× reflective optics. The receiver was assembled in the United Kingdom, using standard electronic processes. All the issues and the challenges faced during the fabrication are reported and discussed in the paper.

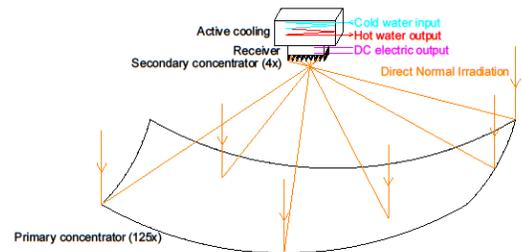


Fig. 1. 3D schematic of the system configuration

II. COMPONENTS, MATERIALS AND FABRICATION

A. The board

A novel, 2.6 kW_p CPV receiver has been developed by the University of Exeter (UK) to be used in 500× applications. It is designed to allocate 144 MJ cells and it is based on a 262.5mm×255.0mm Insulated Metal Substrate (IMS). The distribution of the cells on the substrate fits the secondary concentrators designed by the Indian Institute of Technology Madras (India), where one compound parabolic concentrator, coupled with a homogenizer, is placed onto each cell. The IMS has a 2.003 mm thick 5052 aluminum baseplate and a 70μm-thick copper layer, bonded together with a 4.5 μm thick marble resin. The aluminum base was chosen because of its good balance between thermal performances and costs: it is a good thermal conductor and it is cheaper than copper. Berquist [9] reported that the cost of 3.2mm-thick aluminum is generally equal to the cost of 1.0mm-thick copper. This kind

of substrate has been preferred to a Direct Bonded Copper (DBC) board because of IMS lower costs and good thermal and electrical behavior [10].

The plate was firstly designed in AutoCAD, a computer aided design software developed by Autodesk, and then transferred into a Gerber file. Due to its higher precision compared to mechanical milling, chemical etching was chosen to outline the conductive layer. The insulated metal substrate, shown in Fig. 2, has then been covered by a thin green resistive layer in order to insulate electrically and to protect the conductive layer. The same coating prevents the solder from spreading out of its planned places. The resistive coating need to be opportunely designed to allocate the surface mounted components. The cell's mounting pad layout was increased by 1mm per side compared to the cell surface, in order to take into account the tolerances. The diode's mounting pad layout was designed accordingly to the datasheet.

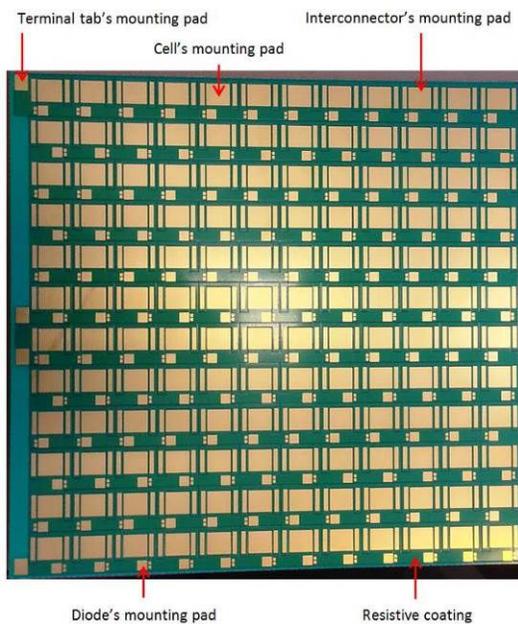


Fig. 2. The bare insulated metal substrate, covered by a thin green electric resistive layer.

B. Soldering of the surface mounted components

The Gerber file included the scheme of a paste mask, to be used to deposit the solder according to the designed pattern. A 0.125mm-thick steel stainless mask was used in this application. The shape of the solder's footprint is a fundamental issue: the presence of voids in the solder can cause hot spots and result in lower performances and damages of the cells [11]. The diode's solder footprint (Fig. 3a) has been designed according to the datasheet, while the cell's solder footprint was split into 9 parts (Fig. 3b), in order to let the solder uniformly distribute under the cell's weight.

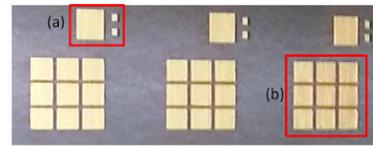


Fig. 3. The solder footprints of three cells (a) and three diodes (b) in series on the paste mask.

A set of 1cm² sized 3C40 cells, provided by Azurspace, has been used in this application. The cells are supplied on a diced wafer and mounted on a tape. These GaInP/GaAs/Ge cells show efficiencies up to 37.2% at 500×, and short circuit currents of 6.587A. Each receiver allocates two 72-cell series: each series is expected to produce 6.444 A at 208V at the maximum power point. A 10A Schottky diode has been coupled with each cell, in order to reduce the power losses and to prevent damages in case of shaded cells. One tin plated brass PCB mount tab terminal has been placed at the starting and the ending points of each series.

The cell's supplier recommended a 3% silver content solder paste: for this reason, a Sn-3.2Ag-0.6Cu solder has been used in this application to paste the surface mounted components (SMC) on the board. The SMC have been manually placed onto the plate, by using a vacuum pick-up system. The dimensions of the board, the low number of boards to be produced and the cells delivered in a diced wafer and mounted on a tape made not possible to use an automatic pick-and-place machine. After the placement of the SMCs, the whole setup was moved into a reflow oven for solder curing. The oven was set at a temperature 217°C, the melting point of the solder. When the oven's atmosphere reached that temperature, the moisture was automatically evacuated and the plate was actively cooled through water jets on the back. A first visual inspection was run.

C. Interconnectors

Micro-welding is the procedure generally exploited by commercial companies to interconnect the front of the cell with the conductive layer [12]: micro-welding grants high mechanical strength to the connection. Wire bonding is a standard micro-electronics technology and it is already exploited as an alternative solution for cell's interconnections [13]. Based on our experience, bonding wires on the small MJ cell's front tabs do not represent a particularly-challenging operation: taking into account the unique CPV features (i.e. the fragility of the cells, the electrical conductivity of the circuit), it can be easily realized even by companies non-specialized in CPV.

Wire bonding generally grants good mechanical strength and high electrical conduction, depending on the materials. Either gold or aluminium wires are generally used. Copper wires have been developed and are gaining much attention, but are not capillary available yet. In our application, 32 μm thick aluminium wires were bonded, because of the higher mechanical strength of aluminium, the lower temperature

required for the bonding process and the lower cost compared to gold. Gold wire bonding requires high temperatures, which are difficult to reach and maintain in such a large aluminium-based board, while aluminium wires can be bonded at room temperature. 32 μm represents one of the most recurrent diameters for aluminium wires. In conditions of shortage of a recognized standard, the minimum number of wires to be bonded on each cell was determined accordingly to the approach suggested by Shah [14]: this method is based on the principle that at steady state all the heat produced by the Joule losses on the wires need to be removed. A number of 50 aluminium wires per cell was found to be necessary to carry the maximum expected current, 6.587 A. The number of wires has been anyway increased for safety reasons: 70 wires per cell have been bonded on the plate to be able to safely face higher currents due to possible wires' failures or inhomogeneous irradiance on the cell's surface.

Before the wire bonding, some solder contamination on the surface of the plate was found (Fig. 5a). Soiling can affect the strength of the wires and enhance the risk of failures during bonding: it has been previously demonstrated that cleaning improves the strength of the bonds [15]. For this reason, a cleaning process was undertaken: the substrate was immersed firstly in DI water, secondly in water and thirdly in a solution of water and DI water. During the whole cleaning the plate was kept in the dark in order to prevent any potential short-circuiting among the subcells. The plate was then dried in a 135°C oven for short time. The effects of the cleaning are clearly shown in Fig. 4.

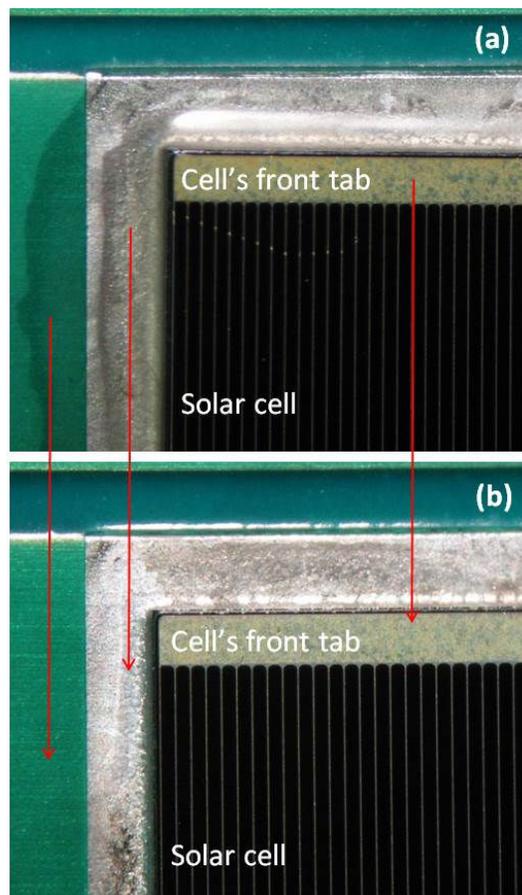


Fig. 4. Comparison between particulars of the pre-cleaning plate (a) and the post-cleaning plate (b).

Wire bonding machine are usually able to handle systems up to 400cm². The considered board goes over this limit, sizing about 670 cm². This means that the machine needs to be stopped time by time, to let the operator move the panel. After that, the machine can be re-threaded, and then started again. According to our experience, the operator needed to take action approximately every 120 wires. Considering 70 wires per device and 144 devices on the plate, it means about 85 human interventions per plate.

D. Encapsulation

During the wire wires bonding, no encapsulation of the interconnectors was attempted, in order not to risk the dark encapsulant to cover part of the cell's active area. An example of encapsulated interconnectors, realized on a previously-developed single cell sample, is shown in Fig. 5. Moreover the size of the board would have made the interconnectors globing more challenging and time-consuming to be realized.

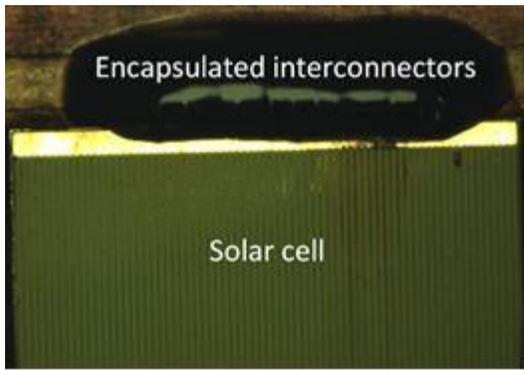


Fig. 5. Example of encapsulated interconnectors

The interconnectors can survive without encapsulation as long as they are not touched, but a transparent encapsulation of the plate was anyway considered essential to reduce the risk of damages to the components, protecting them from external agents and accidental collisions. Sylgard® 184, a clear silicone resin solution produced by Dow Corning, has been used for this duty.

To apply the Sylgard, a frame was built around the plate to stop the coming out of the solution, as shown in Fig. 6. Sylgard was poured as much uniformly as possible across the surface, thick enough to cover all the components and the interconnections. The board was then placed in a vacuum oven for 35 minutes at 100°C. The whole encapsulation process was completed in less than 90 minutes, as per Sylgard datasheet's requirement.

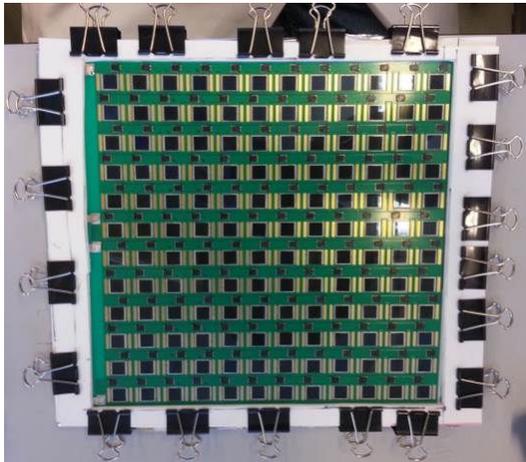


Fig. 6. The frame around the board during the curing of the Sylgard.

III. POST-FABRICATION ISSUES

At the end of the fabrication processes, visual and experimental inspections of the board were carried out. Some wire bond non-sticks were found, as shown in Fig. 7, probably due to contamination on the dies. In the presented system, the 3.75% of the connections are faulty: this means that almost 3

wires per cell are missing, out of 70. A peak of 14 missing wires per cell was counted, with a maximum of 10 wrong connections per cell's side. This remarks the necessity of considering an opportune safety factor while dimensioning the interconnectors: the considered surplus of 20 wires installed on each cell proved to be reliable.

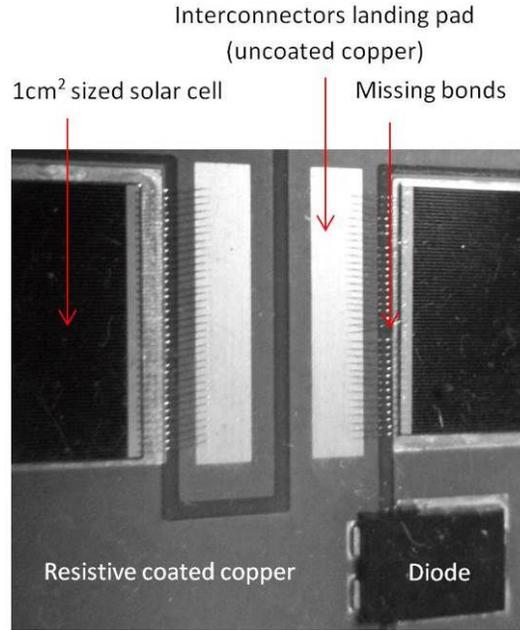


Fig. 7. Some missing wires on a cell's interconnection.

Few weeks after the fabrication, Sylgard was discovered to start peeling off from the edges of the board, endangering the safety of components and interconnectors. Some silicone sealant was then applied on the sides of the encapsulant to stop this phenomenon (red rectangle in Fig. 8). In future, a rigid frame, or an aluminum plate much larger than the copper circuit, may be considered to prevent this occurrence.

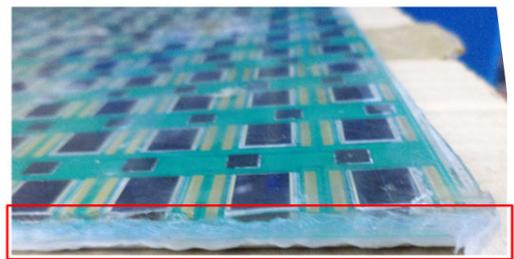


Fig. 8. The silicone sealant on the edge of the board, highlighted in the red square.

IV. CONCLUSIONS

A large, 2.6 kW_p densely packed assembly for 500× CPV applications was developed on an insulated metal substrate as shown in Fig. 9. Due to the large number of cells and the high concentration, the leading issues were to conceive a reliable

and durable receiver able to handle the significant waste heat generation and to grant high electrical properties.

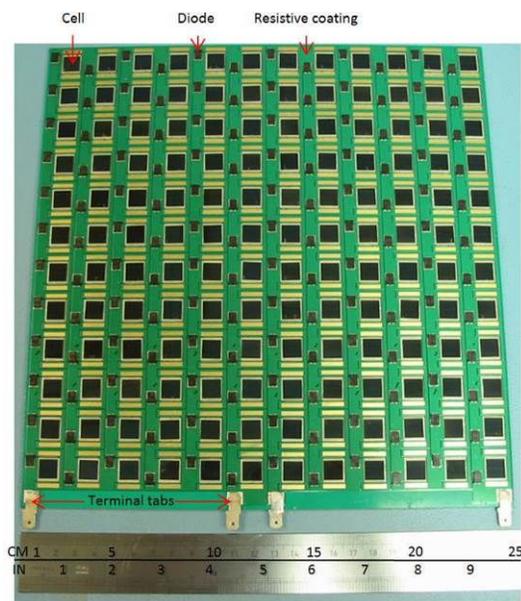


Fig. 9. The completed CPV receiver plate

This work focuses on the whole fabrication process. Although a large number of publications emphasis on the design of new, high efficiency CPV receivers, a lack of information on CPV fabrication was recorded. Manufacturing strongly influences the performance, the durability and the cost of a system, especially in CPV, where requirements for small volumes, high electrical power densities and high heat fluxes meet. A discussion on the CPV production processes would lead to improvement in reliability. The aim of this work is to guide future researchers across the issues and the challenges that can occur while producing a high CPV receiver.

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REFERENCES

[1] A. W. Bett, S. P. Philipps, S. Essig, S. Heckelmann, and R. Kellenbenz, "Overview about Technology Perspectives for High Efficiency Solar Cells for Space and Terrestrial Applications," in *28th European Photovoltaic Solar Energy Conference and Exhibition*, 2013, vol. 0, pp. 1–6.

[2] I. Aeby, D. Aiken, B. Clevenger, F. Newman, P. Patel, T. Varghese, C. Dempsey, G. Flynn, J. Foresi, A. W. Bett, R. D. McConnell, G. Sala, and F. Dimroth, "High Concentration CPV Reliability Progress at Emcore," *Physics (College Park, Md.)*, vol. 229, no. 1, pp. 229–232, 2010.

[3] J. S. Foresi, L. Yang, P. Blumenfeld, J. Nagyvary, G. Flynn, and D. Aiken, "EMCORE receivers for CPV system development," *2010 35th IEEE Photovolt. Spec. Conf.*, pp. 209–212, Jun. 2010.

[4] S. Paredes, W. Escher, R. Ghannam, C. L. Ong, and B. Michel, "Low Thermal Resistance HCPV Multi Chip Receiver for Thermal Energy Reuse," in *28th European Photovoltaic Solar Energy Conference and Exhibition*, 2012.

[5] R. Fucci, C. Cancro, L. Lancellotti, G. Leanza, and C. Privato, "Assembling, Characterization and Energy Rating of a Photovoltaic Concentration Module Equipped with Crystalline Silicon Solar Cells," in *25th European Photovoltaic Solar Energy Conference and Exhibition*, 2010, no. September, pp. 6–10.

[6] J. Nickelsen Jr, P. Je Sung, and G. Pycroft, "Concentrated photovoltaic receiver package with stacked internal support features," *US Pat. 8,502,361*, vol. 1, no. 12, 2013.

[7] D. Fork and D. Duff, "Solar concentrating photovoltaic device with resilient cell package assembly," 2007.

[8] S. Hasin and R. Helfan, "Photovoltaic Module Assembly," US 2013/0319507 A12013.

[9] Berquist Co, "Baseplate Design Considerations." pp. 12–13.

[10] Spirit Circuits Limited, "Requirements of PCB's in solar & LED applications," in *EIPC Winter Conference 2013*, 2013.

[11] G. Calabrese, F. Gualdi, S. Baricordi, P. Bernardoni, V. Guidi, L. Pozzetti, and D. Vincenzi, "Numerical simulation of the temperature distortions in InGaP/GaAs/Ge solar cells working under high concentrating conditions due to voids presence in the solder joint," *Sol. Energy*, vol. 103, pp. 1–11, May 2014.

[12] AZURSPACE Solar Power GmbH, "Enhanced Fresnel Assembly - EFA." 2010.

[13] AUREL s.p.a., "Concentration PhotoVoltaic (CPV): the next generation." .

[14] J. Shah, "Estimating bond wire current-carrying capacity," *Power Syst. Des.*, no. July/August, pp. 22–25, 2012.

[15] P. Hebert, J. Frost, R. Cravens, and R. Woo, "What Not to Do." Sylmar, CA, 2011.